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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/887,035	06/25/2001	Ramkumar Subramanian	039153-0381	7414

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EXAMINER
SAGAR, KRIPA

ART UNIT	PAPER NUMBER
1756	3

DATE MAILED: 12/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N . 09/887,035	Applicant(s) SUBRAMANIAN ET AL.
	Examiner Kripa Sagar	Art Unit 1756

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. Examiner has considered the proprietary information disclosed on 6/25/01. None of the information contained therein has been applied in a rejection.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2-5,15,16,29,30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 2-5, 15,16,29,30 recite the limitation "the step of". There is insufficient antecedent basis for this limitation in the claim. There is no explicit reference to a "step" in the independent claims although, for example, forming a photoresist layer may *imply* a forming step.

This rejection may be overcome by amending the independent claims to read "comprising the steps of:".

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over US PGPUB 2002/0094482 to Mansfield et al. in view of the non-patent publication of Helbert et al. (Handbook of VLSI Microlithography, ch.2). The instant claims recite exposing a photoresist layer to a first mask with dense patterns and a second mask with an isolated pattern, under different exposure settings and patterning the resist and underlying layer. Limitations on resists, feature pitch and etching are recited.

Mansfield teaches most of the elements of claims 1-22.

Mansfield teaches the elements of claim 1 ((#0035). It teaches that wet and dry etching are conventional steps in lithography (#0038). The conventional stacks on a silicon wafer are dielectric layers, semi-conducting layers and conducting layers (#0037). The imaging parameters are adjusted to the mask features; these include partial coherence (sigma) and numerical aperture (NA) (#0035). Mansfield separates the features by their pitch; in one example contact holes with a pitch of 450nm or less (dense) are placed on one mask while those with a larger pitch (isolated) are placed on another mask. This is a predetermined value based on the process design (#0041). Features may be separated into more than two groups and exposed accordingly

(#0042). The masks are exposed according to the process windows for the respective features on the masks (Fig.1,2). The invention is directed towards a semiconductor device made by this process (#0001).

Mansfield does not explicitly teach the development of exposed or unexposed portions of the resist (cl.2,3,14) although it recommends optimizing the resist to the process (#0036). It is well known in the art that photoresists have positive or negative tone; based on the image desired, the exposed or unexposed regions are developed and removed, after exposure with a suitable (brightfield / darkfield) mask. This is taught by Helbert (p74-95)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use positive or negative tone resists and appropriate mask patterns well-known in conventional art, as taught by Helbert in the exposure process taught by Mansfield because Helbert teaches that these are proven materials and that there is a reasonable expectation of successfully forming dense and isolated patterns using these materials.

6. Claim 1 is further rejected under 35 U.S.C. 103(a) as being unpatentable over US Pat6218089 to Pierrat in view of US Pat.5563012 to Neisser.

Pierrat teaches a method of imaging dense and isolated features in IC manufacturing. It teaches that it is conventional to form a photoresist layer on a substrate, expose it to radiation through a mask and to transfer the developed image on to a semi-conductive substrate (1;58-2;6). It teaches diverse methods of patterning

dense and isolated features with improved image fidelity. In one embodiment it teaches exposing a mask with dense and isolated features; first with the illumination settings optimized to image the dense features and a second exposure with the settings for isolated features (4;29-50).

Pierrat teaches overlay exposure with two different masks, but they do not contain features separated according to the pitch (density).

Neisser teaches that features may be grouped according to type or enhancement characteristics (exposure characteristics). The grouped features are placed on different masks and used in multiple overlay exposures; the exposure settings are designed to enhance the particular features. Dense and isolated features are enhanced by different means (2;41-56).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to separate dense and isolated features on to separate masks as taught by Neisser and expose them in sequence as taught by Pierrat because Neisser teaches that this increases pattern fidelity for all features in the composite image compared with that for selected features in conventional techniques (1;36-40).

7. Claims 23-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mansfield in view of US Pat.6309800 to Okamoto.

The claims recite a method of making a semiconductor device on another device layer using dual masks and exposures for dense and isolated features.

The teachings of Mansfield have been discussed above; these cover most of the elements in claims (23-27,31,32). In addition Mansfield teaches that the order of exposure (cl.29-30) of the two masks is not critical to the process (#0034).

Mansfield does not teach forming dense and isolated features atop a device layer (cl.23) or specific materials used in device manufacturing.

Okamoto teaches forming multilayered devices including memory arrays. It teaches forming periodic arrays in the memory portion and isolated features in the peripheral areas. Arrays or of contact holes are featured in the memory cell area. (Fig,7 , 8). The materials used are conventional. The substrate is a semiconductor. The insulating layer is SiO2 or Si-nitride. The conductive material is Al.
The device is a CMOS RAM with poly-Si resistors (28;60-36;9).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the memory cell arrays and peripheral portions of Okamoto's device using multiple exposures with different masks as taught by Mansfield, because Mansfield teaches that it provides flexibility in mask design and increases the process latitude as well as resolution (#0014) in forming contact hole arrays (Fig.3).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US PGPUB 2001/0036604 to Kawashima and US PGPUB 2001/0055733 to Irie et al. both teach imaging dense and isolated patterns using two masks and different exposure settings.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kripa Sagar whose telephone number is 703-605-4427. The examiner can normally be reached on 8:00AM--5:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark F Huff can be reached on 703-308-2464. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9310 for regular communications and 703-872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

MH/ks
December 10, 2002

MARK F. HUFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700